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10/792,208	03/02/2004	Manish K. Ahluwalia	200315296-1	4159

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EXAMINER	
WANG, RONGFA PHILIP	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/792,208	AHLUWALIA ET AL.	
	Examiner	Art Unit	
	Philip Wang	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/2/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detail Action

1. This office action is in response to the application filed on 3/2/2004.

2. Claims 1-47 are pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-47 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 1 recites the limitation "kinds of assertions" in "register which kinds of assertions fail most often" and "analyze the kinds of assertions which fail most often". Per Applicant's specification, page 7, lines 14-15, "... identifying failed assertions by a type and/or kind of assertion in the software code..." It appears that a type (or kind) of assertion is an additional level of abstraction that is different from assertions. So, a type (or kind) of assertion includes more than one assertion. According to the disclosure,

example of assertions are null pointer assertions, locking assertions, and object state assertions (page 14, lines 10-11). In the same paragraph, the disclosure states these assertions "will be known and understood by one of ordinary skill in the art." (page 14, line 12). However, the examiner finds no further explanations of what these assertions are and what types of assertions they belong to.

Claims 12, 25, 32, and 42 recite the limitation of "a kind of assertion" or "types of assertions" that suffer the same deficiency.

Similarly, claims 1 recites the limitation of "analyze the kinds of assertions which fail most often against a set of questions (rules);" According to the specification, pages 13-14,

> In block 420, the method includes analyzing failed assertions against a set of questions, e.g., questions and/or rules applied in the form of computer executable instructions. **One of ordinary skill in the art will appreciate** upon reading this disclosure the manner in which a set of rules and/or questions can be implemented as computer executable instructions.

It appears that the disclosure repeatedly stating "One of ordinary skill in the art will appreciate upon reading this disclosure..." However, the examiner does not observe further detailed information regarding how this desired function is being implemented.

Claims 12, 24, 32, 39, 44 recite the limitation of analyzing or correlating failed assertions against a set of rules that suffer the same deficiency.

Claims 2-11 depend on claim 1; claim 13-23 depend on claim 12; claims 25-31 depend claim 24; claims 33-38 depend on claim 32; claims 40-43 depends on claim 39; claims 44-47 depend on claim 43, therefore suffer the same deficiency.

Claims 4, 15, 29, recite the limitation of "null pointer assertions, locking assertions, and object state assertions. According to the specification, page 14, lines 11-12 "null pointer assertions, locking assertions, and object state assertions as the same will be known and understood by one of ordinary skill in the art." However, the examiner does not observe further detail regarding what these assertions are. The specification appears to state a list of desired assertions without further providing any detained information.

Claims 5, 16, 27, recite the limitation of "execute to register assertions which fail as received from hardware and software components selected from the group of: a compiler; a debugger; a test controller; and an integrated development environment (IDE). " According to the specification, page 13, lines 24-29, "Various embodiments can include registering assertions which fail as received from a compiler, a debugger, a test controller, and/or an integrated development environment (IDE), among other hardware and/or software/firmware components." The specification appears to state a list of desired functions without giving details regarding how the limitation is implemented. Assertions are well known to be used during program run time. However, for example,

to enable assertion during compile time, the steps and functions required for such implementation are lacking in the specification.

4. Claims 1-47 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1 recites the limitation "kinds of assertions" in "register which kinds of assertions fail most often" and "analyze the kinds of assertions which fail most often". Per Applicant's specification, page 7, lines 14-15, "... identifying failed assertions by a type and/or kind of assertion in the software code..." It appears that a type (or kind) of assertion is an additional level of abstraction that is different from assertions. So, a type (or kind) of assertion includes more than one assertion. According to the disclosure, example of assertions are null pointer assertions, locking assertions, and object state assertions (page 14, lines 10-11). In the same paragraph, the disclosure states these assertions "will be known and understood by one of ordinary skill in the art." (page 14, line 12). However, the examiner finds no further explanations of what these assertions are and what types of assertions they belong to. Claims 12, 25, 32, and 42 recite the limitation of "a kind of assertion" or "types of assertions" that suffer the same deficiency.

Claims 2-11 depend on claim 1, claim 13-23 depend on claim 12, claim 26 depends claim 25, claims 33-38 depend on claim 32, claim 43 depends on claim 42, therefore suffer the same deficiency.

Similarly, claims 1 recites the limitation of "analyze the kinds of assertions which fail most often against a set of questions (rules);" According to the specification, pages 13-14,

> In block 420, the method includes analyzing failed assertions against a set of questions, e.g., questions and/or rules applied in the form of computer executable instructions. **One of ordinary skill in the art will appreciate** upon reading this disclosure the manner in which a set of rules and/or questions can be implemented as computer executable instructions.

It appears that the disclosure repeatedly stating "One of ordinary skill in the art will appreciate upon reading this disclosure..." However, the examiner does not observe further detailed information regarding how this desired function is being implemented.

Claims 12, 24, 32, 39, 44 recite the limitation of analyzing or correlating failed assertions against a set of rules that suffer the same deficiency.

Claims 2-11 depend on claim 1; claim 13-23 depend on claim 12; claims 25-31 depend claim 24; claims 33-38 depend on claim 32; claims 40-43 depends on claim 39; claims 44-47 depend on claim 43, therefore suffer the same deficiency.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation of "the assertions" in "score the assertions". There is insufficient antecedent basis for this limitation in the claim.

Claims 2-11 depend on claim 1 and suffer the same deficiency.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-47 are rejected under 35 U.S.C. 102(e) as being anticipated by Blementhal et al. (US PGPub. No. 2005/0055605).

As per claim 1,

Blumenthal et al. disclose

- a processor; a memory coupled to the processor; and program instructions provided to the memory and executable by the processor to:
- register which kinds of assertions fail most often during testing of software code; analyze the kinds of assertions which fail most often against a set of questions (rules); and score the assertions which fail ([0057], "...a count of the number of failures...").

As per claim 2,

the rejection of claim 1 is incorporated;

Blumenthal et al. disclose

- further including program instructions which execute to collect a history of assertions which fail in a system under test ([0007], "...log status on assertion failure...").

As per claim 3,

the rejection of claim 1 is incorporated;

Blumenthal et al. disclose

- further including program instructions that execute to assign points to the assertions which fail ([0057], "...a count of the number of

failures…").

As per claim 4,

the rejection of claim 1 is incorporated;

Blumenthal et al. disclose

- wherein the assertions include assertions selected from the group of: null pointer assertions; locking assertions; and object state assertions([0007]).

As per claim 5,

the rejection of claim 1 is incorporated;

- further including program instructions that execute to register assertions which fail as received from hardware and software components selected from the group of: a compiler; a debugger; a test controller; and an integrated development environment (IDE)(see Figure 1).

As per claim 6,

the rejection of claim 1 is incorporated;

Blumenthal et al. disclose

- further including program instructions that execute to collectively analyze assertion failures across a number of systems under test ([0065], "A

computer program can be deployed to be executed on one computer or on multiple computers at one site or distributed across multiple sites and interconnected by a communication network.").

As per claim 7,

the rejection of claim 1 is incorporated;

Blumenthal et al. disclose

- further including program instructions that execute to identify types of assertions which fail([0057], "...a count of the number of failures...").

As per claim 8,

the rejection of claim 1 is incorporated;

Blumenthal et al. disclose

- further including program instructions that execute to automatically generate feedback on identified types of assertions which fail across different systems under test to improve application of assertions in a coding process([0068], "...feedback provided to the user...").

As per claim 9,

the rejection of claim 1 is incorporated;

Blumenthal et al. disclose

- further including program instructions that execute to correlate an instance of a failed assertion with a type of assertion ([0057], "...a count of the number of failures...").

As per claim 10,

the rejection of claim 1 is incorporated;

Blumenthal et al. disclose

- wherein the device is connected to a system under test, wherein the system under test includes a computing device connected to a local area network (LAN) having software code executing thereon ([0065], "A computer program can be deployed to be executed on one computer or on multiple computers at one site or distributed across multiple sites and interconnected by a communication network.").

As per claim 11,

the rejection of claim 1 is incorporated;

Blumenthal et al. disclose

- wherein the device is connected to a system under test, wherein the system under test includes a computing device connected to a wide area network (WAN) ([0065], "A computer program can be deployed to be executed on one computer or on multiple computers at one site or distributed across multiple sites and interconnected by a communication network.").

As per claim 12,

Blumenthal et al. disclose

- A software testing system, comprising: a computing device having software code executing thereon; and a software testing device coupled to the computing device, the software testing device, comprising: a processor; a memory coupled to the processor; and program instructions provided to the memory and executable by the processor to: register assertions which fail in association with the software code executing on the computing device; analyze assertions which fail against a set of rules

to determine a kind of assertion which repeatedly fails; collect a history of assertions which fail in association with the software code executing on the computing device; and score the assertions which fail ([0057], "...a count of the number of failures..."; [0007], "...log status on assertion failure...").

As per claims 13-17,

- they recited the same limitation of claims 9, and 3-6, therefore are rejected for the same reason set forth in connection of the rejection of claims 9, and 3-6 above.

As per claim 18,

the rejection of claim 17 is incorporated;

Blumenthal et al. disclose

- further including program instructions that execute to: collect a history of assertions which fail in association with the software code executing on the number of computing devices connected to the software testing device; and correlate assertion failures according to one or more types of assertions in the software code executing on the number of computing devices connected to the software testing device ([0007], "...log status on assertion failure...").

As per claim 19,

the rejection of claim 12 is incorporated;

Blumenthal et al. disclose

- further including program instructions that execute to automatically generate feedback on identified types of assertions which failed in the software code executing in an integrated development environment to improve application of assertions in a coding process ([0047], "...user can view the trace output..."; [0068], "...feedback provided to the user...").

As per claim 20,

the rejection of claim 19 is incorporated;

Blumenthal et al. disclose

- further including program instructions that execute to generate a report identifying one or more failed assertions by instance of failed assertion type([0047], "...user can view the trace output...").

As per claim 21,

the rejection of claim 20 is incorporated;

Blumenthal et al. disclose

- further including program instructions that execute to transmit the report, identifying one or more failed assertions by instance of failed assertion type, to a developer of the software code([0047], "...user can view the trace output...").

As per claim 22,

the rejection of claim 12 is incorporated;

Blumenthal et al. disclose

- further including program instructions that execute to register and analyze various failures which are not represented by assertions in association with the software code executing on the computing device (see Figure 1, where a debugger register and analyze various failures).

As per claim 23,

the rejection of claim 22 is incorporated;

Blumenthal et al. disclose

- further including program instructions that execute to; collect a history of the various failures which are not represented by assertions in association with the software code executing on the computing device; and score the

various failures in association with the software code executing on the computing device according to a failure type ([0057], "...a count of the number of failures...").

As per claim 24,

Blumenthal et al. disclose

- A method for software testing, comprising: registering assertions which fail during testing of software code; analyzing failed assertions against a set of questions; and scoring failed assertions based on analyzing failed assertions against a set of questions ([0057], "...a count of the number of failures...").

As per claim 25,

the rejection of claim 24 is incorporated;

Blumenthal et al. disclose

- wherein the method includes registering which types of assertions fail most frequently during testing of software code ([0057], "...a count of the number of failures...").

As per claim 26,

the rejection of claim 25 is incorporated;

Blumenthal et al. disclose

- wherein the method includes collecting a history of assertions which fail in a system under test(see rejection of claim 2).

As per claim 27,

the rejection of claim 24 is incorporated;

Blumenthal et al. disclose

- wherein the method includes registering assertions which fail as received from hardware and software components selected from the group of: a compiler; a debugger; a test controller; and an integrated development environment (IDE)(see rejection of claim 5).

As per claim 28,

the rejection of claim 24 is incorporated;

Blumenthal et al. disclose

- wherein the method includes assigning points to the assertions which fail(see rejection of claim 3).

As per claim 29,

the rejection of claim 24 is incorporated;

Blumenthal et al. disclose

- wherein the method includes registering failed assertions selected from the group of: null pointer assertions; locking assertions; and object state assertions(see rejection of claim 4).

As per claim 30,

the rejection of claim 24 is incorporated;

Blumenthal et al. disclose

- wherein the method includes analyzing assertion failures across a number of systems under test(see rejection of claim 6).

As per claim 31,

the rejection of claim 24 is incorporated;

Blumenthal et al. disclose

- wherein the method includes: registering various failures which are not represented by assertions during testing of software code; analyzing the various failures against a set of questions; collecting a history associated with the various failures; and scoring the various failures according to a failure type based on analyzing the various failures against a set of questions (see rejection of claim 23).

As per claim 32,

Blumenthal et al. disclose

- A method for software testing, comprising: registering assertions which fail in association with software code executing on the computing device; analyzing assertions which fail against a set of rules to determine a kind of assertion which repeatedly fails; collecting a history of assertions which fail in association with the software code executing on the computing device; and scoring the assertions which fail ([0057], "...a count of the number of failures...").

As per claim 33,

the rejection of claim 32 is incorporated;

Blumenthal et al. disclose

- wherein the method includes correlating assertions which fail with a type of assertion in the software code executing on the computing device (see rejection of claim 9).

As per claim 34,

the rejection of claim 32 is incorporated;

Blumenthal et al. disclose

- wherein the method includes collectively analyzing assertion failures in association with software code executing on a number of computing devices in a system under test(see rejection of claim 6).

As per claim 35,

the rejection of claim 34 is incorporated;

- Blumenthal et al. disclose

  wherein the method includes: collecting a history of assertions which fail in association with the software code executing on the number of computing devices; and correlating assertion failures according to one or more types of assertions in the software code executing on the number of computing devices(see rejection of claim 18).

As per claim 36,

the rejection of claim 35 is incorporated;

Blumenthal et al. disclose

- wherein the method includes correlating assertion failures in an integrated development environment to improve application of assertions in a coding process(see rejection of claim 5).

As per claim 37,

the rejection of claim 35 is incorporated;

Blumenthal et al. disclose

- wherein the method includes: generating feedback based on correlating assertion failures according to one or more types of assertions; and

identifying one or more failed assertions by instance of failed assertion type(see rejection of claim 8).

As per claim 38,

the rejection of claim 35 is incorporated;

Blumenthal et al. disclose

- wherein the method includes transmitting report information, identifying one or more failed assertions by instance of failed assertion type, to a developer of the software code (see rejection of claim 21).

As per claim 39,

Blumenthal et al. disclose

- A computer readable medium having instructions for causing a device to perform a method, comprising: registering assertions which fail during testing of software code; analyzing failed assertions against a set of questions; and scoring failed assertions based on analyzing failed assertions against a set of questions ([0057], "...a count of the number of failures...").

As per claim 40,

the rejection of claim 39 is incorporated;

Blumenthal et al. disclose

- wherein the method includes collecting a history of assertions which fail (see rejection of claim 2).

As per claim 41,

the rejection of claim 40 is incorporated;

Blumenthal et al. disclose

- wherein the method includes registering assertions, analyzing failed assertions, scoring failed assertions, and collecting a history of assertions which fail across a number of software code tests(see rejection of claim 6).

As per claim 42,

the rejection of claim 41 is incorporated;

- wherein the method includes correlating assertions which fail with one or more types of assertions in the number of software code tests(see rejection of claim 9).

As per claim 43,

the rejection of claim 42 is incorporated;

- wherein the method includes transmitting report information, identifying one or more failed assertions by instance of failed assertion type, to a developer of the software code(see rejection of claim 19).

As per claim 44,

Blumenthal et al. disclose

- A software testing device, comprising: a processor; a memory coupled to the processor; and means for correlating assertions which fail with one or more types of assertions in a number of software code tests being conducted by the device ([0057], "...a count of the number of failures...").

As per claim 45,

the rejection of claim 44 is incorporated;

Blumenthal et al. disclose

- wherein the means for correlating assertions includes a set of program instructions which execute to track failed assertions and to register a type of assertion in software code associated with a particular failed assertion ([0057], "...a count of the number of failures...").

.As per claim 46,

the rejection of claim 44 is incorporated;

Blumenthal et al. disclose

- wherein the device further includes program instructions provided to the memory and executable by the processor to collect a history of assertions which fail across the number of software code tests(see rejection of claim 2).

As per claim 47,

the rejection of claim 44 is incorporated;

Blumenthal et al. disclose

- wherein the device further includes program instructions provided to the memory and executable by the processor to transmit report information, identifying one or more failed assertions by instance of failed assertion type, to a developer of the software code(see rejection of claim 43).

Conclusion

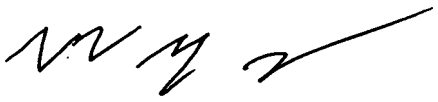
The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

It is noted that any citation [[s]] to specific, pages, columns, lines, or figures in the prior art references and any interpretation of the references should not be considered to be limiting in any way. A reference is relevant for all it contains and may be relied upon for all that it would have reasonably suggested to one having ordinary skill in the art. [[See, MPEP 2123]]

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Philip Wang whose telephone number is 571-272-5934. The examiner can normally be reached on Mon - Fri 8:00AM - 4:00PM. Any inquiry of general nature or relating to the status of this application should be directed to the TC2100 Group receptionist: 571-272-2100.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Zhen can be reached on 571-272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



WEI ZHEN
SUPERVISORY PATENT EXAMINER